B1

to chip set 220. Memory controller 300 may read data from, and write data to, main memory 213. For some operations such as main memory refresh, memory controller 300 must access all portions of main memory 213 within a deterministic time period. According to one embodiment, memory controller 300 is included within chip set 220.

Please replace the paragraph beginning at page 10, line 4 with the following paragraph:

B2

Refresh unit 320 is coupled to refresh timing unit 330 and recharges electrical cells within main memory 213 in order to maintain data integrity. Refresh unit receives a REFRESH signal from refresh timing unit 330 in order to trigger a refresh event. Refresh unit 320 also receives a power status signal (STAT) from bus bridge 240. STAT is an indicator of whether computer system 200 is operating in a normal mode or a low power mode. The low power mode of operation enables power conservation whenever computer system 200 is powered up, but has not recently been used. Additionally, refresh unit 330 receives HOST CLK from processor 205.

Please replace the paragraph beginning at page 11, line 17 with the following paragraph:

B3

According to one embodiment, clock generator 836 is a ring oscillator implemented using a chain of thirty-seven (37) serially coupled inverters. The OSCLK signal is generated each time a signal completely propagates through the chain of inverters. One of ordinary skill in the art will appreciate that clock generator 836 may be implemented using other quantities of inverters. Further, other clock

generation methods may be used to implement clock generator 836.

Please replace the paragraph beginning at page 14, line 14 with the following paragraph:

At process block 520, a subsequent memory refresh is triggered by host clock counter 834. As described above, memory refreshes are triggered every 15.6 microseconds. At process block 530, the incremented count (i.e., the number of OSCLK pulses received by counter 434 between normal refresh cycles) is transmitted to buffer 436 as VALUE. At process block 540, counter 434 is again reset after the refresh, and control is returned to process block 510 wherein counter 434 begins counting OSCLK pulses again. According to one embodiment, the normal mode operation of refresh timing unit 330 is continually repeated in order to periodically update the number of OSCLK pulses that occur during a refresh cycle. Consequently, timing refresh unit continuously tracks the number of OSCLK pulses that occur between memory refreshes whenever it is operating in the normal mode.